Review UDK 004.42
doi: 10.7251/COMEN1702196O

MAGNETORESISTIVE RANDOM ACCESS MEMORY

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Abstract: For decades, the memory hierarchy was determined based on latency, bandwidth, and cost between processors, random access memory (RAM), and secondary memory. Although the gap between the processor and RAM has been dampened by fast cache memory, the gap between RAM and secondary memory has remained challenging, expanding to 12 size range in 2015 and continuing to expand by around 50% per year. The rapid development of nanotechnology has triggered a new field in the organization of memory space. For more than a decade, FRAM - ferro random access memory has been in use, which keeps data in the form of a polarization of the ferroelectric crystal that does not lose polarization after the power is turned off. The real revolution is expected in the use of magnetic resonance random access memory (MRAM), which represents data storage technology using magnetic moments, not electric charges. Unlike conventional RAM chips, data in MRAM are not stored as an electrical charge, but with magnetic storage elements. The advantage of this memory is energy independence, that is, the storage of recorded data and the absence of power supply. MRAM has similar properties as SRAM, similar to the density of the record as dynamic RAM (DRAM), with much less consumption, and in relation to flash, it is much faster and with time does not degrade its performance. Theoretically, there is no limit to the number of read and write, so new memories could last unlimited. The paper will discuss this new type of memory organization.

Keywords: RAM; FRAM; SSD; FLASH; FeRAM; MRAM; STT-MTJs; TORQUE-SPIN.

1. INTRODUCTION

The effects of magnetoresistance date back to 1850 when Lord Kelvin showed that the application of a magnetic field to a metal object increases the electrical resistance of the object in one direction and reduces it in the direction of the normal. Since then, several other types of magnetoresistance have been discovered. The most important papers were written by Alberto Ferta and Peter Grunberg, who received the Nobel Prize in Physics 2007 for discovering the GMR effect, which has been used for magnetic field sensors applied in modern computer magnetic disks of extremely high capacity. They claimed that the maximum values of electrical conductivity under the external magnetic field are obtained when the cells have a width of 3 nm to 5 nm, with vacuum bulkheads of 1 nm to 3 nm between them. However, they also noticed that the tunneling of electrons between cells depends on the relative orientation of the magnetization direction on adjacent cells and the external magnetic field. In addition, they found that electrical conductivity is maximized when the magnetic moments in adjacent cells are parallel-oriented, leading to the effect of tunnel magnetoresistance (TMR). The value of tunnel magnetoresistance essentially depends on the properties of the insulating material between these cells. Based on these discoveries, of course with the development of science and nanotechnology, there is a possibility of applying and developing a new kind of memory. Magnetoresistive Random-Access Memory is a permanent magnetic-resistant RAM random access memory that belongs to the NVRAM memory submenu. So far, two technologies have been commercially available in magnetic disks and NVRAMs [1]. In the paper, we will observe a potentially useful and applicable device in the future - MRAM. Magnetic memories were used in the first computers sometime until 1975. But they were not forgotten, as the researchers continued to search for a way to perfect them. At that time, it was the only material that enabled the permanent storage of data and the implementation of memory for writing and

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reading. It seems that the time has come for the massive application of MRAM [2,3]. The biggest advantage of this type of memory is that it stores data even after power failure, so it is used wherever data loss is unacceptable. Solid State Drive has a similar feature, but they have two major drawbacks: the time of writing is very long and the number of entries is limited. In many embeded systems, FRAM is already widely used. Unlike the SSD, where the number of entries ranges from 5000 to 100,000, depending on the technology of production, the number of cycles in this memory is greater than 100,000,000,000,000, which makes them virtually eternal. Writing time is almost 1000 times shorter than in flash memory (SSD) [3] and the consumption is considerably lower, Table 1.

Table 1. Characteristics of the memory circuit

	CHARACTERISTIC				REQUIREMENT		
	ST-MRAM	3D Xpoint	Resistive RAM	Low Power CBRAM	SSD Buffer	RAID Buffer	Server Write Cache
Supplier	Everspin	Intel/Micron	Crossbar	Adesto			
Latency R/W	10ns / 20ns	50ns / 1us	100ns / 100us	50ns / 1us	<100ns	<80ns	<70ns
Endurance	10^{10} - 10^{12}	10^6 - 10^7	10^5 -10^6	10^5	10^9-10^{11}	10^{11}	10^{11}- 10^{13}
Interface	DDR3/ DDR4	Proprietary	Flash Like	SPI	DDR3/4	DDR3/4	DDR3/4
Status	Shipping 64Mb	Sampling	R+D	Production			
Density	Gb	64Gb+	Tb potential	64Mb	256Mb-4Gb	1Gb-4Gb	1Gb-8Gb

As SSD continue to push the envelope in terms of system performance and smaller form factors, SSD solution providers are facing greater challenges to increase density, endurance, performance and add significant new functionality while continuing to protect data from power failures. Next generation SSD will rapidly grow to 32TB and beyond by using more flash channels with faster interface speeds, and higher density flash devices. If a traditional architecture of a controller with DRAM working memory is employed, this significantly increases the need for energy storage for power fail protection which in turn reduces space available for the storage array for a fixed form factor. These next generation devices will also require new functionality including advanced CMB buffering, in-line encryption, deduplication and compression.

A flash solid state drive (SSD) is a non-volatile storage device that stores persistent data in flash memory. There are two types of flash memory, NAND and NOR. The names refer to the type of logic gate used in each memory cell. (Logic gates are a fundamental building block of digital circuits). NOR flash was first introduced by Intel in 1988. NAND flash was introduced by Toshiba in 1989. The two chips work differently. NAND has significantly higher storage capacity than NOR. NOR flash is faster, but it's also more expensive. Flash has an internal „insulation“ layer that can hold an electric charge without external power. This is what makes it non-volatile, but writing to NAND flash requires a relatively large „charge pump“ of voltage, which makes it slower than RAM and eventually wears it out. In order to accomplish this, a power fail detection and isolation circuit, that includes hold up energy storage, works in conjunction with logic in the SSD controller to flush all volatile data not committed to the nonvolatile array in the event of a power failure. Because of the relatively slow write speed, NAND Flash, the controller and memory system must be held up for hundreds of milliseconds.

A Solid State Drive (SSD) has three key components: controller, volatile DRAM working memory and nonvolatile flash memory array, Figure 1. Because of the limitations of flash performance and endurance, a number of advanced algorithms are needed to manage the flash array to create a robust storage subsystem. These algorithms include garbage collection, error correction and wear leveling. The controller is an embedded processor that manages accesses to the flash array through the use of these algorithms. The DRAM working memory is necessary to buffer reads and writes from the host as well as to enable quick access to the flash translation table (FTL) and metadata.

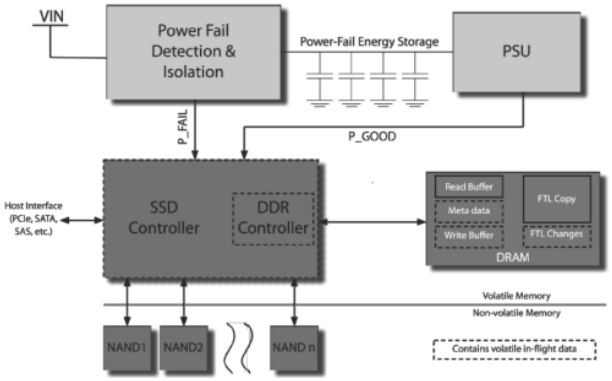


Figure 1. SSD Architecture

This memory does not require deleting a segment between two entries. Certain characteristics of memory devices should be a measure of comparison with all existing and new technologies that we anticipate in the future. Of course, the basic criteria on the basis of which we will make comparisons are: capacity, the size of the cell, access time and price.

2. MRAM

Perhaps the most promising technology today is a type of nvRAM based on magnetoresistance. Magnetoresistive random-access memory (MRAM) stores information as a magnetic orientation rather than as an electrical charge. This immediately provides a much higher reading and writing performance

that is much closer to DRAM speeds than flash because bits are read by testing with voltage, not current, and written with a small current boost, not a huge charge [4].

However, in certain applications, the importance of electricity consumption should not be ignored. MRAM has so far found application in the Del Storage Systems, in BMW racing cars, Siemens production automation devices, as well as in Airbus's flight controllers. To describe today's status of this technology, we can see that Motorola demonstrated a 1-Mbit MRAM chip using a 0.6-μm process, defining a cell size of 7.2μm^2. Anticipations are that the use of 0.18-μm technology will reduce a cell size to 0.7μm^2, which is already comparable to flash memory. Sony demonstrated the MRAM chip using a 0.35-μm technological process, defining the cell size of 5.8μm^2. Other companies like IBM in partnership with Infineon are also very active in MRAM research. Figure 2 shows the development of these memory modules. What makes the MRAM memory extraordinary is the ability to build a new hierarchical architecture of memory devices, where the main memory and cache L2, L3 will be stored in it.

After several decades of continuous scaling of the Moore law, it now seems that conventional silicon-based devices are approaching their physical limitations. In today's deep submicro circuits, numerous channels and quantum effects are appearing that affect the production process, as well as the functionality of microelectronic systems on the chip. Besides the basic electronic charge, magnetic resonance random access memory and spintronic devices that exploit both the internal spin of an electron and its accompanying magnetic moment promise solutions to circumvent these threats. Compatible with CMOS technology, such devices offer acceptable synergy from radiant immunity, endless endurance, stability, increased packing density, etc. In this paper, we present a magnetic MRAM cell that is able to store and process data both electrically and magnetically. The cell is based on perpendicular magnetic tunnel junctions (STT-MTJs) and can be used in magnetic random access memory and reprogrammable computers (persistent registers, processor cache memory, magnetic field programmable logic circuits, etc.).

The mode of operation could be described in a simplified way: data is stored in magnetic cells, consisting of two mutually insulated ferromagnetic panels. One plate is a permanent magnet, while in the second polarity is changed, Figure 3, to the left. Reading is performed by measuring the electrical resistance of the cell. If both plates have the same polarity, the resistance is smaller and this is interpreted as logical „1“, if the polarities are different, the resistance is greater and that is interpreted as „0“. The researchers developed various technologies for the development of MRAM [5]. Figure 3 on the right represents the overview of the MRAM field, indicating a fully selected bit (arrows and central position) and 1 < 2 selected bits along each of the write-off lines. When turning on - MRAM, all bits are oriented at 45 degrees with respect to the lines of writing. Simultaneous impulse flows in two control lines are required to shift the magnetization of the free layer in relation to their cross-section, but control is also needed to prevent errors if a switch with only one impulse occurs. It is reported that these random access memory fields have been produced up to 4 Mb.

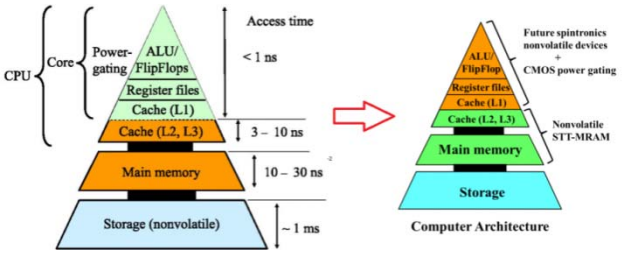


Figure 2. New hierarchical architecture of memory devices and technologies

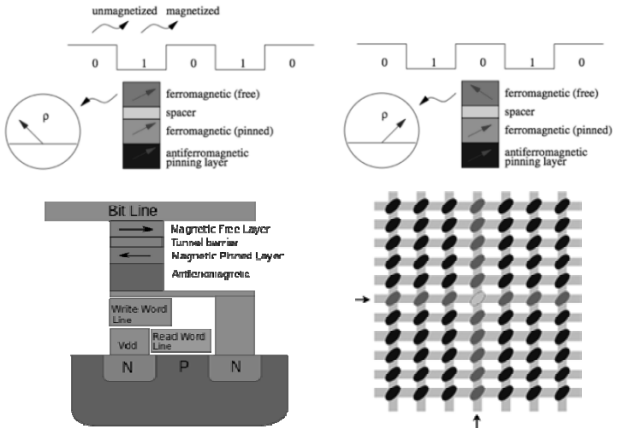


Figure 3. Basic elements of the MRAM system and bit orientation

Memory cells cannot yet be reduced to the same extent as in DRAM memory, so MRAM still has a smaller capacity. But the capacitors in the DRAM need to be refreshed at least twenty times per second, with the content of the cell being read and rewritten, so that energy is constantly consumed during operation. MRAM is only used for writing and reading data, without the need for refreshment. Energy savings depend on the application, that is, how often information is changed, but some say that savings can be up to 99%. With this, MRAM is a serious candidate for operation in mobile devices, thus extending the battery life and reducing the size of the memory space.

The simplest way of reading is achieved by measuring the electrical resistance of the cell. A specific cell is (usually) selected by supplying a transistor that transfers power from the supply line through the cell to the ground. Due to magnetoresistance and tunneling, the electrical resistance of the cell changes due to the relative orientation of the magnetization in two plates. By measuring the resulting current, resistance can be determined within any particular cell, and therefore the polarity of the magnetization of the recording plate. Typically, if the two plates have the same magnetization position (low resistance state), this is considered logical „1“, whereas if the alignment is anti-parallel the resistance will be higher (high resistance state), which means logic „0“.

Another advantage is the speed of access to data. IBM researchers have achieved a speed of 2ns, which is faster than DRAM. German scientists from the Physikalisch - Technische Bundesanstalt demonstrated the speed of 1ns, but only on one cell. In terms of flash memory, writing is several thousand times faster.

MRAM is comparable to SRAM, or Static RAM, which consists of transistors that store one of two states. And it gets high speed with low power consumption, but as four or six transistors are used in one cell, the SRAM memory is expensive. It is used mainly as cache memory in today's processors.

The proponents argue that MRAM has similar properties like SRAM and similar density of records as DRAM, but with much lower consumption. In relation to flash, it is much faster and does not degrade over time. Allegedly, there is no limit to the number of reading and writing, so new memory (theoretically) could last infinitely.

When shutting down, computers should not store data on secondary memory devices, but simply turn off power, so that when switched on again, they would recover everything as it was before the shutdown state. There would be no long-term processes that we call boot and shutdown. All this, according to MRAM advocates, could allow MRAM to become „universal memory“. But the high cost of investing in the construction of production facilities makes manufacturers to be cautious, so they are still supplying the market with the traditional memory that are still looking for their customers.

Ferroelectric random access memory (FeRAM, FRAM) and magnetospheric or magnetic random access memory (MRAM) are commercially available as new and fast memory for various electronic data storage systems.

A few hundred million FeRAM embedded chips have been shipped around the world since the second half of the nineties. Mass production of MRAM chips started in 2006. A large number of papers and research are carried out in this part of science and technology in terms of materials for their creation up to their architecture.

Figure 4 shows the key components and mechanisms for data storage of FeRAM and MRAM devices. The ferroelectric capacitor shown in Figure 4 (a) is used as a FeRAM memory cell. Two remanent polarization directions in the ferroelectric film of the capacitor create two memory states. The polarization direction is switched using the controlled voltage between the electrodes. Remanent polarization is caused by the movement of atoms causing ferroelectricity. The stored data are read by detecting the polarization of the change in the current of the ferroelectric capacitor when the reading voltage is brought between the electrodes.

Parallel or antiparallel magnetization, Figure 4 (b), of two ferromagnetic films on either side of the insulator (tunnel barrier) of the magnetic tunnel compound represent different memory states. The direction of the magnetization of the ferromagnetic film changes the magnetic field induced by current through the wiring or by transmitting the torque spin induced by a current through the MTJ (Magnetic Tunnel Junction) [6,7]. The tunnel resistance between ferromagnetic films is low for parallel magnetization and is large for antiparallel magnetization. The stored data are read by recognizing the change in the tunnel current caused by the effect of magnetoresistance.

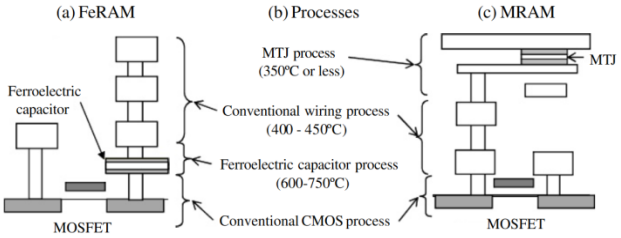


Figure 4. (a) A ferroelectric condenser formed around the MOSFET and (b) MTJs located at the top

MRAM is based on a magnetic tunnel joint (MTJ), Figure 5. Key features of MRAM technology are a very fast reading / writing operation, low-voltage operation, non-destructive reading, unlimited reading and writing continuity. 16-Mbit standard MRAM and 1-Mbit embedded MRAMs have already been developed.

The maximum memory capacity of a standard MRAM is 4 Mbits. It is used in standard NVRAM and replaces the built-in SRAM. Technical issues include memory capacity (scalability), reading margin and writing current.

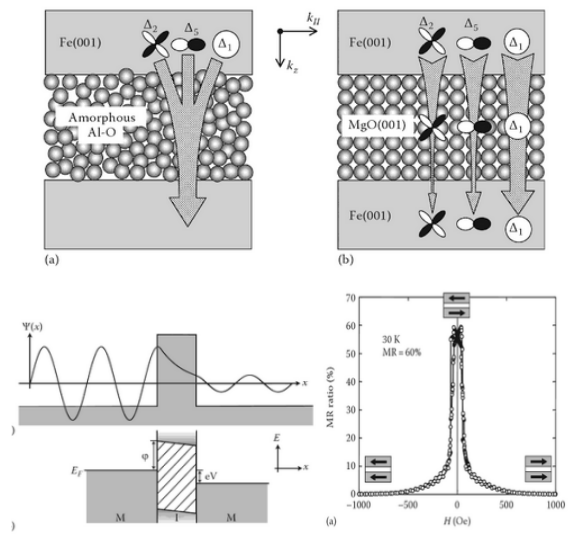


Figure 5. Schematic representation of the tunneling of the electron through a) the amorphous AlO barrier and b) the crystalline MgO (001) barrier c) the energy of the excitation required for tunneling d) the magnetoresistant curve at 30K through the epitaxial Fe (001) / Mgo (001) / Fe (001) layer

Figure 6 shows the basic structure of the magnetic tunnel compound (MTJ) for the circuit of the memory cell MRAM. MTJ is composed of a free ferromagnetic layer, a thin (1 ~ 2 nm) insulator (tunnel barrier), added ferromagnetic layer and an antiferromagnetic layer, [8,9].

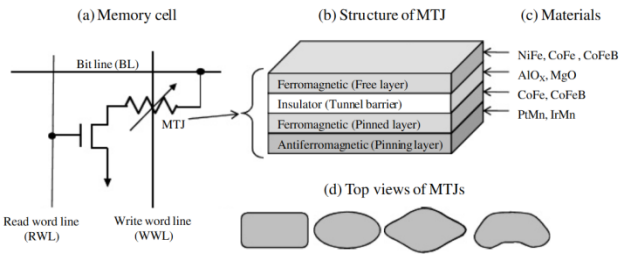


Figure 6. (a) Memory cell, (b) tunneling magnetic coupling (MTJ), (c) materials, (d) top view of MTJs for MRAM

Data is stored according to the direction of magnetization of the free layer in the magnetic tunnel joint. Different types of MTJ have been developed to improve reading / writing characteristics. The stored data are read by changing the tunneling current due to the effect of magnetoresistance.

When the free-layer magnetization direction and the added layer direction are the same, that is parallel, the tunnel resistance is low. When the magnetization directions are contrary to each other, namely anti-parallel, the tunnel resistance is high. Lately, the synthetic antiferromagnetic structure (SAF) is used for the bonded layer and / or free layer of MTJ, as shown in Figure 6. The structure of the SAF is formed of two ferromagnetic layers (CoFeB) separated by a non-magnetic separation layer (Ru). The dependence of the polygon field is reduced by using a free layer with the SAF structure.

In an MTJ [9], the two electrodes are ferromagnetic materials. In a ferromagnetic material, an electric current consists of two partial currents, each with either spin-up or spin-down electrons. In a tunneling process in which electron spin is conserved, the tunneling conductance depends on whether the magnetizations M1 and M2 of the two electrodes are parallel or antiparallel. When the relative magnetization orientations are at an angle Θ, the conductance becomes proportional to cosΘ as:

$$G(\Theta =)\frac{1}{2}(G_P + G_{AP}) + \frac{1}{2}(G_P - G_{AP})cos\Theta \quad (1)$$

where G_{AP} and G_P are the conductance for θ= 180° (when the two moments are antiparallel, AP) and θ= 0° (when the two moments are parallel, P), respectively.

The corresponding tunneling magnetoresistance (TMR) ratio is defined as:

$$TMR\ ratio = \frac{G_P - G_{AP}}{G_{AP}} = \frac{R_{AP} - R_P}{R_P} \quad 2)$$

where RAP and RP are the resistances in the antiparallel and parallel state, respectively.

Using the definition of TMR ratio given by equation:

$$TMR\ ratio = \frac{2P_1P_2}{1-P_1P_2} \quad (3)$$

where P_1 and P_2, defined below, are the polarization factors for the two electrodes, respectively. The polarization factors are defined as:

$$P = \frac{N_\uparrow(E_F) - N_\downarrow(E_F)}{N_\uparrow(E_F) + N_\downarrow(E_F)} \quad (4)$$

The magnetoresistant (MR) ratio can be represented by the following formulas:

$$TMR\ ratio(\%) = 100 \times (R_{AP} - R_P)/R_P. \quad (5)$$

The MR ratio depends on the ferromagnetic and insulating material and has a major impact on the amount, speed and scalability of MRAM. When the AlOX film is used as an MTJ insulator (tunnel barrier), the MR value is less than 100%. However, a large MR ratio was obtained using the MgO film instead of the AlOX film as an insulator. MTJ with 230% MR ratio was developed using a (100) -orbed mono crystalline MgO film deposited on amorphous CoFeB by atomizing, [9].

The use of the MgO film significantly improves the reading margin of MRAM, Figure 7.

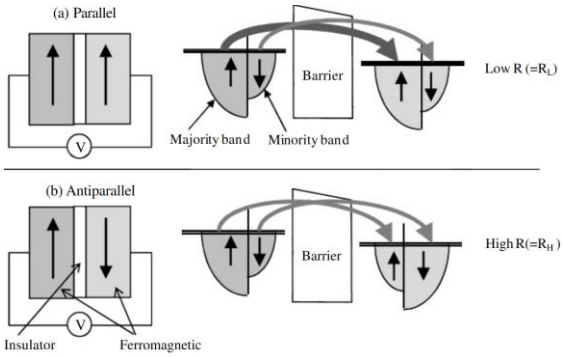


Figure 7. Effect of magnetoresistance. (a) The electron current is tunneled from the major layer to the major layer when the magnetization directions are parallel. (b) The electron current is tunneled from the major layer to the minor layer when the magnetization directions are antiparallel

When two conducting electrodes are separated by a thin dielectric layer with a thickness ranging from a few angstroms to a few nanometers, electrons can tunnel through the dielectric layer (often referred to as the tunnel barrier) resulting in electrical conduction. As illustrated in Figure 7, the electron tunneling phenomenon arises from the wave nature of the electrons while the resulting junction electrical conductance is determined by the evanescent state of the electron wave function within the tunnel barrier. The evanescent transmission of electrons through the tunnel barrier leads to the exponential dependence of the tunneling current with the barrier thickness, as given by the expression. Figure 7 is a graphic illustration of the various parameters used in the equation:

$$I(V) = f(t_b)\left(\left(\overline{\Phi} - \frac{V}{2}\right)e^{-\left(1.025\sqrt{\overline{\Phi}-\frac{V}{2}}\right)t_b} - \left(\overline{\Phi} + + \frac{V}{2}\right)\right)e^{-\left(1.025\sqrt{\overline{\Phi}+\frac{V}{2}}\right)t_b} \quad (6)$$

where I is the tunneling current, θ and V are the average tunnel barrier height and bias voltage across the junction in volts, respectively, and t_b is the barrier thickness in angstroms.

3. MEMORY CELL

Three basic memory cells have been developed to reduce the memory area and increase the performance of MRAM, as shown in Table 2. There have recently been suggested a variety of memory cells such as 2T1MTJ86 or 1T2MTJ87. 1T1MTJ cells are used in commercially available MRAMs. The 2T2MTJ memory cell consists of 2 transistors and 2 MTJs [10,11].

Table 2. Characteristics of the memory cell circuit

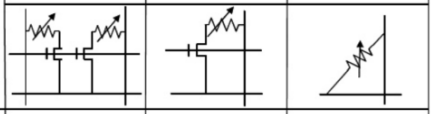
	Memory cell area: Large ← → Small		
	2T2MTJ	1T1MTJ	Cross point
Memory cell circuit			
Access time	>2 ns	>5 ns	>250 ns
Write current/MTJ	0.1 - 10 mA		4 mA
MR (magnetoresistance) ratio	10 - 70% (AlO_X based MTJ), >100% (MgO based MTJ)		
Data retention	>10 years		
Read/Write endurance	Unlimited		

Table 2 shows 2T2MTJ consisting of two 1T1MTJs and works at high speed. ThebMTJ writing current is too large for the MRAM-built SoC (system on the chip) because it simultaneously accesses a large number of embedded memory cells.

The data and the opposite data are written in two MTJs simultaneously. Data are read by comparing the current of two MTJs. The 2T2MTJ memory cell has a larger memory cell area and a higher reading resolution than the 1T1MTJ memory cell, as well as the ratio between 2T2C and 1T1C in FeRAM. The cross point memory cell has the smallest memory area in all MRAMs.

4. MRAM OPERATIONS

In Figure 8, an MRAM writing operation is performed, which is executed with two orthogonal magnetic fields generated by the current flow through the bit line (BL) and the write word line (WWL). The writing operation is done correctly when the magnetic fields, Hk and Hi are in the switching areas. There is no change in the region that has not been stirred. BL and WWL writing streams should be in the region of transit regions to ensure the MTJ's escape. This means that the writing margin of MRAM is small [10−12].

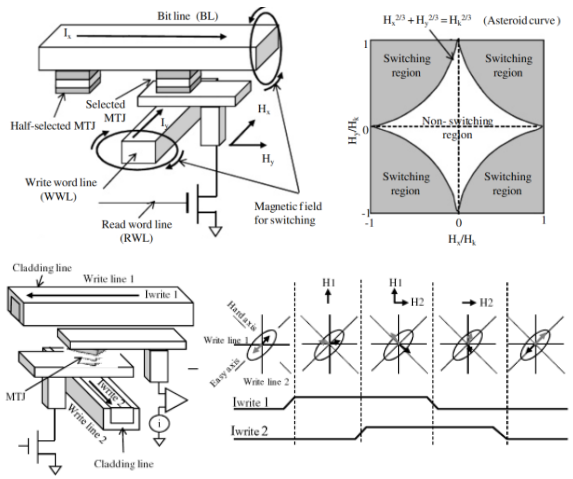


Figure 8. The switching current is increased rapidly by reducing the dimensions of MTJ

The switching field, which generates the current of the record, strongly depends on the size of the MTJ, as shown in Figure 8. The diamagnetic field increases as the size of the MTJ decreases and the writing current increases.

The free layer of MTJ consists of a balanced multilayer SAF, which is formed over two ferromagnetic layers separated by a non-magnetic connection of the layer connecting these anti-parallel layers. The MTJ axis is aligned in the middle of the angle between the two orthogonal line of writing (it enters lines 1 and 2). Two phase pulse sequences are applied to rotate the direction of magnetization of the free layer of SAF by 180 degrees. A writing string translates the magnetic state to the opposite state regardless of the existing state, Figure 9. Therefore, pre-read is used to determine if a data record is required. The data stored in the MTJ is changed from „0“ to „1“ or „1“ to „0“ whenever the two-phase writing of the pulse sequence is applied.

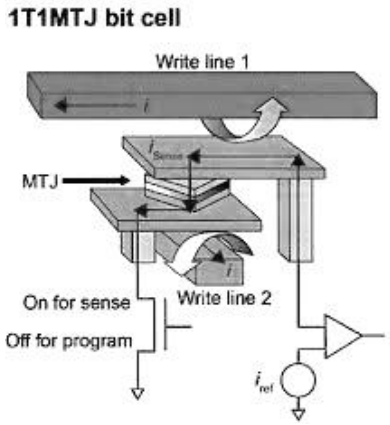


Figure 9. The technology of reading and writing data

5. MRAM OPERATION OF READING

Figure 10 shows the operation of reading MRAM devices. The stored data are read through the characteristic resistance of MTJ. The amplitude of the reading signal depends on the relationship between magnetoresistance (MR) and tunnel resistance. MRI size also decreases when applied voltage to MTJ increases. MRAM with high reading margin must have precise control of insulator thickness and readout voltage, [13,14].

Schematic of an MRAM memory element array is shown in Figure 11. For the toggle MRAM design, the long axis of the elliptically shaped element is oriented diagonally with respect to the x-y grid of writing lines. Each memory element is connected to a designated transistor, which performs the function of reading selection [14].

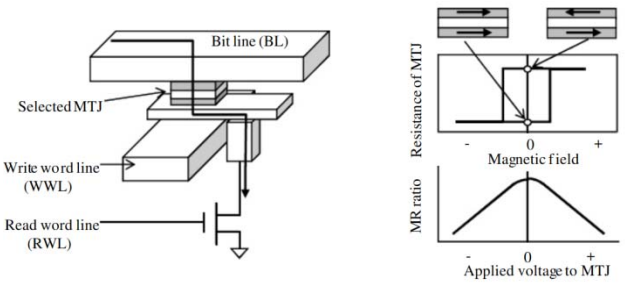


Figure 10. Reading operation of the selected MTJ

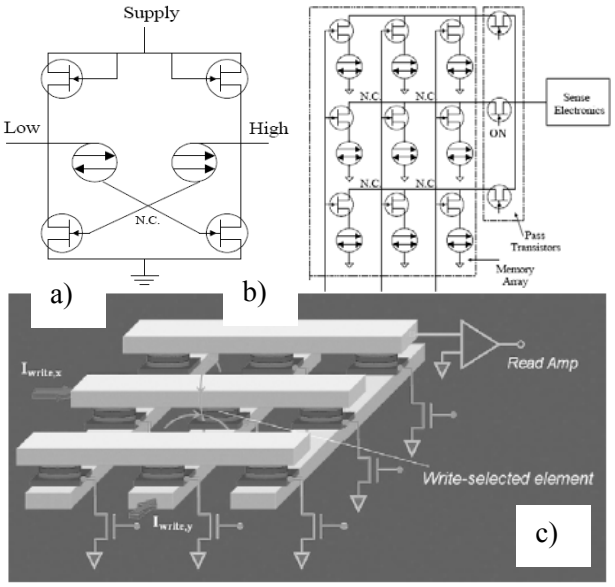


Figure 11. a) Static RAM Cell, b) 3x3 Array of SDT Memory Cells. C) Schematic of an MRAM memory element array

A recent success has been reported in the field of magnetic logic devices, a class called quantum cellular automata (KCA), based on interactions of nanomagnets. The current devices are extremely promising, because they work at room temperature and are simple in concept and production. The basic idea is clear from Figure 12, taking into account the nature of the dipole magnetic field, as shown by the conventional magnet.

Figure 12 shows the scheme of the universal logical gate of the magnetic point. The central nanomagnet chooses its magnetization direction (up or down, due to its elongated shape) based on the magnetic field sum of similar input nanomagnets 1, 2, and 3. The output is simply anti-parallel against the central magnet and thus represents a negative majority input. This is a simple magnetostatics, whose dipole magnetic fields lead to the anti-parallel direction of magnetization of the neighborhood in the x direction, and parallel (ferromagnetically) close to the neighbor in the direction y. The only quantum aspect that appears in this situation is a complex quantum effect for the formation of ferromagnetic domains, [15].

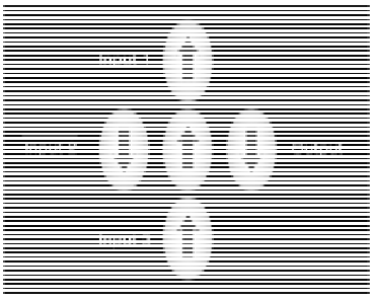


Figure 12. The appearance of magnetic dipoles in MRAM

The table shows the sum of logical states on most gateways for all input combinations (Truth table). The logical state of the central nanomagnet determines the logical majority state of its three input neighbors, of which the ferromagnetically connected neighbors „vote“ directly and the antiferromagnetically connected neighbors „vote“ in reverse in relation to their magnetic state [16]. The logical state of the central magnet is inverted to the output magnet by the antiferromagnetic compound. If the programming is done using the values of the first input bit, the majority gate can function as a double input NAND gate (upper four rows of the table) or as an input NOR gate (lower four rows of the table), Figure 13.

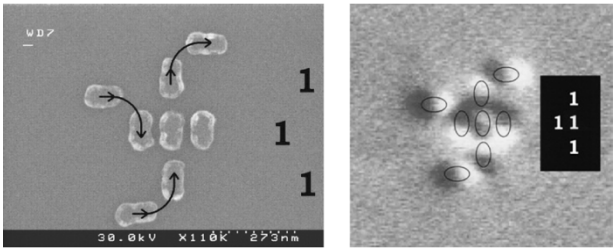


Figure 13. TEM (Transmission Electron Microscopy) images of planar nanomagnets with nominal dimensions of 135 nm and 70 nm with 30 nm Permalloy film thickness

The horizontal distance between the (vertically elongated) nanomagnets is 25 nm. Horizontally oriented magnets on the left are drivers, and those on the right read the output. The external pulse field B regulates the magnetic direction of the magnetization. It is suggested that the magnetization time (magnetization or selection) in the nanometer scale of the magnetic point is about 100 ps. It is stated that this logical gate would have an operating speed of 100 MHz, with a dissipation of energy (heating) of about 1 eV per switching event.

Based on this, a series of 1000 gateways would have a total dissipation of 0.1 eV, assuming that each device is switched once per cycle. This is followed by a truth table for NAND and NOR gateways, Table 3:

Table 3. Thruth table of the Logical state

Input magnet	Central magnet	Output magnet
000	0	0
001	0	0
010	0	0
011	1	1
100	0	0
101	1	1
110	1	1
111	1	1

The new magnetoresistant effect binds four-state memory devices, Figure 14.

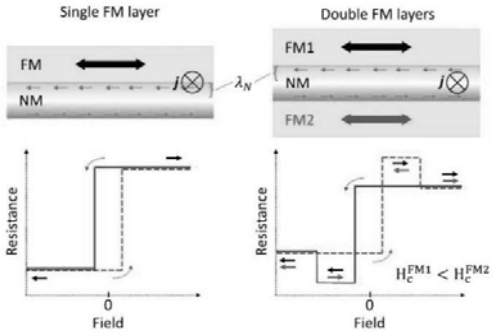


Figure 14. Magnetic-resistant MRAM memory with four states

Figure 14 (left)- a single ferromagnetic layer, system has two levels of resistance (right). Adding another ferromagnet to the system gives four levels of resistance, which corresponds to four different magnetic states indicated by arrows. In 2015, scientists have discovered a new effect of magnetoresistance - that is, a new way in which magnetization affects the electrical resistance of materials, but usable applications for this discovery that is beyond existing technologies have not yet been found. Now in the latest research, the same scientists have shown that the effect can be used to design a memory cell with four different stable magnetic states, allowing the memory to store four bit information in one magnetic structure and many more bits, all in comparison to the simple upgrade of the memory device.

In 2015, scientists have discovered the latest magnetoresistance effect, called spin Hall single-magnetoresistance [17−20]. This effect differs from other types of magnetoresistance because the change in resistance depends on the direction of both magnetization and electrical current. Based on the research, it was found out that this effect depends on the direction, since the spin-polarized electrons formed by the spin Hall effect in the non-magnetic layer are deflected in the opposite directions by magnetization of the adjacent magnetic layer.

Earlier this new effect was demonstrated in two-layer structures consisting of a non-magnetic and magnetic layer. But, adding another magnetic layer, researchers have achieved a great potential advantage for memory organization: the ability to distinguish not only two but four magnetic states. In spite of the fact that it is possible to have four different magnetic states, other types of magnetoresistance effects are only sensitive to the relative orientation of the magnetization (parallel or antiparallel). Since the new effect is sensitive to the direction of the magnetization of individual layers, then there is a possibility to establish the difference between all four magnetic states, Figure 15.

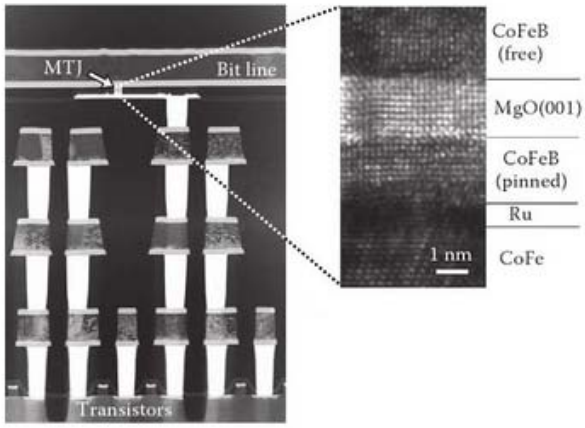


Figure 15. Magnetic-resistant MRAM with spin. TEM image 4k bit Spin RAM memory by capturing eB / MgO / CoFeB MTJ_a (Courtesy of Sony Corp., Tokyo, Japan)

It has been experimentally confirmed, in a three-layer structure, that it is possible to achieve four different levels of resistance, which would correspond to four different magnetic states. In this way, it has been shown that four levels of resistance can be read by simple electrical measurements, opening the way for the development of an electric multi-bit-per-cell memory device.

Based on this, it can be expected that by adding more layers, this memory device will drastically increase the bit density, which would allow as many as eight different magnetization states, each with its unique resistance level. Further improvement of these memory devices can be achieved by applying materials that exhibit a higher one-way effect of spin magnetoresistance.

6. CONCLUSION

Although very simple by their purpose, data storage and memory devices were developed much more slowly than processors. Unlike the processor which (by 2002) doubled the speed and number of elements every two years (about 41% per year), the main memory advanced only 5-7% per year. In addition, no media has enabled the implementation of data storage devices which will have high writing and reading speed at the same time, high capacity and low cost of stored data, while continuing to be permanent (not to lose content after switching off the power supply).

In order to achieve all these characteristics, it is necessary to use various technologies and materials, i.e. realization of the hierarchy of memory devices: registers, cache (L1, L2, L3), work memory, temporary storage of data (realized in semiconductor technology) and secondary memory for permanent storage of data (realized primarily on magnetic materials, but also semiconductor and optical materials).

FRAM, and in particular MRAM memory, allow for the practical realization of all the features that a storage device should possess: speed, capacity, durability, hence over time, the price of the stored data will become acceptable. This is, of course, closely related to the increase in their application, which will lead to mass production and reducing prices. Especially in this sense, significant is MRAM, or magnetoresistant memory with arbitrary access. This paper presents a magnetic MRAM cell that is able to store and process data both electrically and magnetically. The cell is based on perpendicular magnetic tunnel junctions (STT-MTJs) and can be used in magnetic random access memory and reprogrammable computers (persistent registers, processor-cache memory, magnetic field programmable logic circuits, etc.)

7. REFERENCES

[1] H. Haidari, *MRAM, the Next Storage Memory a non-volatile memory*, Flash Memory Summit Proceeding, Vol.1 (2013) 2013814_204A_Haidrai.pdf, Santa Clara, CA, USA.

[2] I. L. Prejbeanu, M Kerekes, Ricardo C. Sousa, J P Nozì Eres, *Thermally assisted MRAM*, Journal of Physics Condensed Matter, Vol. 19−16 (2007) 26.

[3] W. Reohr, H. Hoenigschmid, R. Robertazzi, D. Gogl, F. Pesavenot, S. Lammers, K. Lewis, C. Arndt, Y. Lu, H. Viehmann, R. Scheuerlein, L.K. Wang, P. Trouilloud, S.Parkin, W. Gallagher, and G. Mueller, *Memories of Tomorrow*, IEEE Circuits &Devices, Vol. 18 (2002) 17–27.

[4] B. Dieny, R. B. Goldfarb, K. J. Lee, *Introduction to Magnetic Random-Access Memory*, John Wiley & Sons, Book Chapter 6, NY USA (2016), 165−188.

[5] J. M. Slaughter, R. W. Dave, M. De Herrera, M. Durlam, B. N. Engel, J. Janesky, N. D. Rizzo, S. Tehrani, *Fundamentals of MRAM Technology*, J. Superconductivity: Incorporating Novel Magnetism, Vol. 15 (2002) 19−25.

[6] S. Yu, P. Y. Chen, *Emerging Memory Technologies: Recent Trends and Prospects,* IEEE Solid-State Circuits Magazine,Vol. 8−2 (2016) 43–56.

[7] M. D. Stiles, J. Miltat, *Spin Transfer Torque and Dynamics, in Spin Dynamics in Confined Magnetic Structures*, III: Topics in Applied Physics 101, eds. B. Hillebrands and A. Thiaville, Berlin: Springer, 2006, 225−308.

[8] G. D. Fuchs et al., *Spin Transfer Effects in Nanoscale Magnetic Tunnel Junctions*, Applied Physics Letters, Volume 85, Issue 7, NY 11747−4300, USA, (2004).

[9] Jagan Singh Meena, Simon Min Sze, Umesh Chand and Tseung-Yuen Tseng, *Overview of emerging nonvolatile memory Technologies*, Nanoscale Research Letters, SpringerOpen Journal, Vol. 9−526 (2014) 1−33.

[10] P. Le Clair, J .T. Kohlhepp, H. J. M. Swagten, W. J. M. de Jonge, *Interfacial density of states in magnetic tunnel junctions*, Phys. Rev. Lett., Vol. 86 (2001) 1066–1069.

[11] J. L. Griffen, S. W. Schlosser, G. R. Ganger, D. F. Nagle, *Operating System Management of MEMS-based Storage Devices*, Carnegie Mellon University, Research Showcase @ CMU, Pittsburgh, PA, USA, 2000.

[12] S. A.Wolf, D. Treger, A. Chtchelkanova, *Spintronics: The Future of Data Storage*?, Mrs Bulletin, Vol. 31 (2006) 400−403

[13] H. A. Engel, L. P. Kouwenhoven, D. Lossand, C. M. Marcus, *Controlling Spin Qubits in Quantum Dots*, Quantum Information Processing, Vol. 3/1–5(2004).

[14] *High-Reliability Read-Method for Spin-Torque-Transfer MRAM, Next-Generation Non-Volatile Memory*, Phys.Org, February 12, Fujitsu, 2010.

[15] V. Khvalkovskiy, D. Apalkov, S. Watts, R. Chepulskii, R. S. Beach, A. Ong, X. Tang, A. Driskill-Smith, W. H. Butler, P. B. Visscher, D. Lottis, E. Chen, V. Nikitin, M. Krounbi, *Basics principles of the STT - MRAM cell operation in memory arrays*, Journal of Physics D: Applied Physics, Vol. 46−7 (2013) 139601.

[16] J. Daughton, *Magnetoresistive Random Access Memory (MRAM)*, Thin Solid Films, Vol. 216 (1992) 162−168.

[17] N. D'Souza, J. Atulasimha, S. Bandyopadhyay, *Four-state nanomagnetic logic using multiferroics*, Journal of Physics D: Applied Physics, Volume 44−26 (2011) 265001.

[18] L. Jiang, W. Wen, D. Wang, L. Duan, *Improving read performance of stt-mram based main memories through smash read and flexible read*, 21st Asia and South Pacific Design Automation Conference (ASP-DAC), Vol 1 (2016) 31–36.

[19] H. J. M. Swagten, *Spin tunneling in magnetic junctions*, In: Buschow K H J (ed.) *Handbook of Magnetic Materials*, Elsevier, Vol. 17, Chap. 1 (2007) 1–121.

[20] W. J. Gallagher, S. S. P. Parkin, *Development of the magnetic tunnel junction MRAM at IBM: From first junctions to a 16-Mb MRAM demonstrator chip*, IBM J.Res. & Dev., Vol. 50 (2006) 5−23.

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МАГНЕТНООТПОРНА МЕМОРИЈА СА СЛУЧАЈНИМ ПРИСТУПОМ

Сажетак: Деценијама се меморијска хијерархија утврђивала на основу латенције, ширине пропусног опсега и трошкова који настају између процесора, RAM-а и секундарне меморије. Иако је јаз између процесора и RAM-а ублажен брзим кеш меморијама, јаз између RAM-а и секундарне меморије остао је непремостив, проширивши се на 12 редова величине у 2015. години и настављајући се ширити за око 50% годишње. Брзи развој нанотехнологије покренуо је једно ново поље у организацији меморијског простора. Више од деценије у употреби су FRAM меморије са случајним приступом, које податке чувају у облику поларизације фероелектричног кристала који не губи поларизацију након искључења напајања. Права револуција се очекује у примјени магнетноотпорних меморија са случајним приступом (MRAM), која представља технологију чувања података помоћу магнетских момената, а не електричних набоја. За разлику од конвенционалних технологија RAM чипа, подаци у MRAM-у се не меморишу као електрични набој, него помоћу магнетских складишних елемената. Предност ове меморије је енергетска независност, односно чување записаних подата-

ка и без присуства напајања. MRAM има слична својства као SRAM, сличну густину записа као DRAM, уз много мању потрошњу, а у односу на flash много је бржа и са временом не деградирају њене перформансе. Теоретски, не постоји ограничење броја читања и писања, па би нове меморије могле трајати неограничено. У раду је било ријечи о овој новој врсти организације меморије.

Кључне ријечи: меморија са случајним приступом RAM, FRAM, FeRAM, SSD, FLUSH, Магнетоотпорна RAM, ћелија са магнетним тунелским спојевима STT-MTJs , спин обртног момента.